FPGA: Advanced Timing Analysis with TimeQuest

HILF!GmbH Microcomputer-Consulting, Hofoldingerstr. 16 a, 82054 Sauerlach bei München Tel.: +49 (8104) 9085 250, Fax: +49 (8104) 9085 251
Web: www.hilf.de
Email: info@hilf.de

Target Group

Hardware engineers who develop FPGAs and would like to enhance their skills, in order to acquire better expertise with TimeQuest, and be able to write constraints for advanced interfaces

Previous Knowledge

Some experience with FPGA design and TimeQuest

Course Description

This advanced course goes into great depth and touches upon writing timing constraints for high speed and advanced interfaces such as SDR, DDR, LVDS, as well as clock and data feedback systems.
The course teaches how to write timing constraints directly into an SDC file rather than using the GUI and then enhance the constraint file using TCL constructs, and perform timing analysis through the use of TCL scripts.
The course also covers timing analysis methodology, and how to achieve timing closure.
The course combines 50% theory with 50% practical work in every meeting.

The practical labs cover most of the theory and also include practical digital design.

This course also enriches digital engineers with many years of experience.

Course Material

• Course Notes

Course Goals

1. Write TCL script files to automate constraining and analysis of FPGA designs

2. Apply timing exceptions to real design situations

3. Properly constrain and analyze the following design situations: source synchronous interfaces, external feedback designs, and high speed interfaces containing dedicated SERDES hardware

4. Apply recommended timing analysis methodology for design timing closure

5. Become familiar with advanced options in TimeQuest

Development Tools:
Synthesizer and Place & Route: Quartus II (ALTERA)